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Impact of Interface traps and Parasitic capacitance on Gate Capacitance of $In_{0.53}Ga_{0.47}As$-FinFET for sub 14nm technology node

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ABSTRACT

FinFET technology has emerged to be one of the advanced nanoscale devices for Moore's Law. The presence of several parasitic components in FinFET has significant effect on the device performance for the channel length of the order 14 nm. The III-V materials are replacing Silicon in FinFET technology to overcome the challenges faced by Silicon. The III-V compound semiconductors material such as Indium Gallium Arsenic (InGaAs), when used as channel material with high-K dielectric oxide materials faces a critical problem of interface traps. In this paper, the significance of interface traps at different energy levels was analysed in 14 nm InGaAs FinFET at high-k/InGaAs channel material. Apart from, the interface traps the gate parasitic capacitance of FinFET with channel material of InGaAs beyond 14 nm gate length was also investigated.

Keywords: FinFET, InGaAs, Interface Traps and Parasitic Capacitance.

1. INTRODUCTION

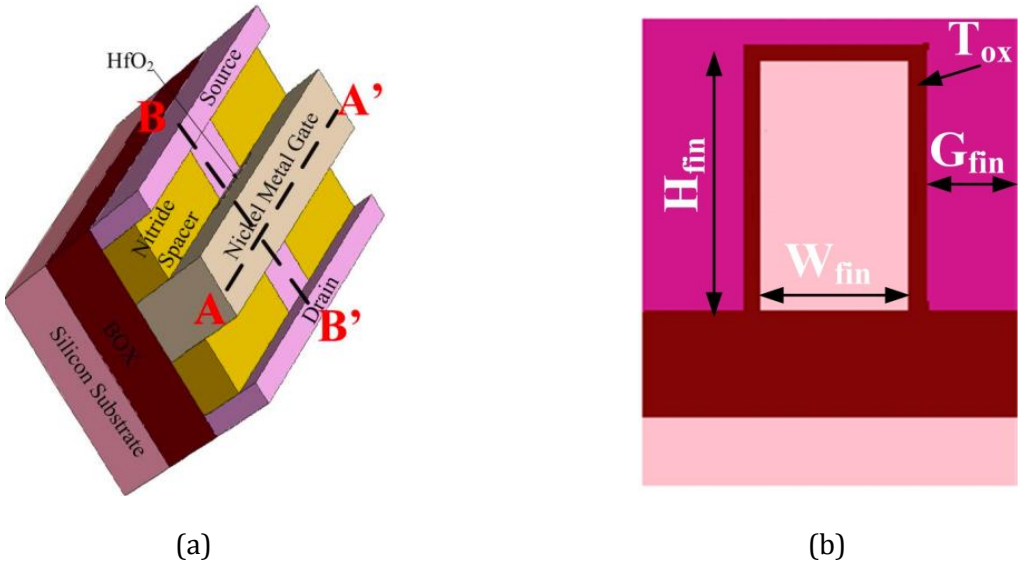
Over the elapsed several decades, size reduction of Complementary Metal Oxide Semiconductor (CMOS) circuits has empowered the microelectronics industry. The bulk planar FET is facing severe challenges for scaling beyond the 32 nm node as many of the scaling advantages are disappearing. The transition from planer FET to 3-D devices gives better control over short channel effects (SCEs), electrostatic control and also raises the performance of devices [1] FinFET (Fin Field Effect Transistor) is coming forward to be a suitable candidate with the reduction in channel length and other dimensions of the devices [2] [3]. With continuous scaling silicon is facing challenges for low power circuits and high-speed applications, such as low electron mobility. So to overcome these problems III-V materials are the best replacement. InGaAs is III-V semiconductor compound can be the alternate material of silicon.

FinFETs are now more scalable than planer MOSFETs. The circuits with InGaAs based CMOS technology provides high speed and low power for many analog and digital applications. While considering InGaAs channel based FinFET, the parasitic components reduce the performance of the device. The presence of gate parasitic components affects the device performance significantly.. Due to this, the overall circuit performance especially the speed of operation gets degraded. The modelling of gate parasitic components for Si based FinFETs is well established [4],[5],[6]. The same modelling techniques are used to simulate parasitic components of FinFET fabricated using InGaAs as the channel material. The parasitic capacitance observed in the device is generally fringing capacitance. The fringing capacitance increases while moving towards structures like FinFETs which then affects the overall gate capacitance and influences the delay of the device. Another aspect which affects the InGaAsFinFETs is the interface traps. InGaAs has low DOS (Density of States) and it is because of the low effective mass. The gate capacitance of FinFET is depended on inversion charge capacitance and oxide capacitance. The low DOS in InGaAs channel material affects inversion charges in the device which results in the reduction of overall gate capacitance. The gate capacitance can only be adjusted through oxide capacitance. The use of high-k oxides on III-V semiconductor can provide high oxide capacitance but with some challenges like high interface traps. There are several high-k oxides like Al_2O_3, HfO_2, Zr_2O_3, Si_3N_4, TiO_2 etc. which are used extensively with III-V semiconductor compounds [7],[8]. However, these oxides exhibit higher D_{it} (interface traps density) with InGaAs material.

In FinFET beyond 14 nm, these parameters have a significant impact. This makes it very important and interesting to study the effect of these parameters on InGaAsFinFET. In the present work the gate parasitic capacitance and interface traps for 14 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET are studied.

The entire paper is outlined as follows: section 2 describes the device development in detail, section 3 contains the method to extract gate parasitic capacitance and analysis of interface traps in $In_{0.53}Ga_{0.47}As$ FinFET which is followed by the results and discussion in section 4 and the paper concludes in section 5.

2. MATERIAL DESCRIPTION



(a) (b)

Figure 1: FinFET structure (a) 3-D view (b) cross section view along A-A'

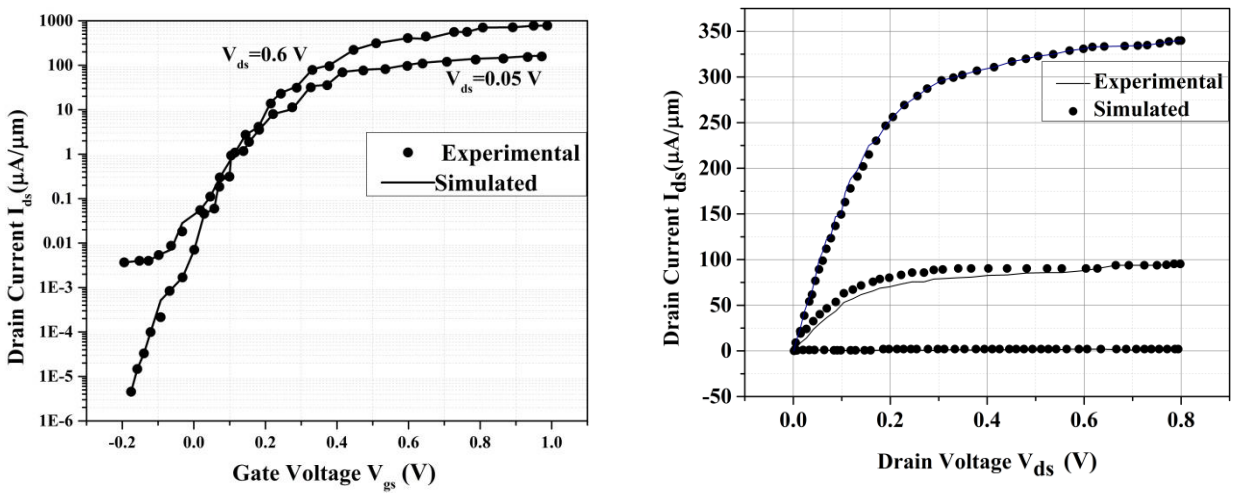
The detailed structure parameters in this paper are prescribed from 2013 ITRS (International Technology Roadmap for Semiconductors)[9]. Table **1** reflects the dimensions of structure for channel length of 14 nm.A combination of InGaAs/$HfO_2$was taken as oxide/semiconductor interface; several techniques have been successfully implemented to integrate HfO_2 on InGaAs [10]. The body was doped with beryllium of concentration $10^{17}cm^{-3}$, while S/D was doped with silicon of concentration $5x10^{19}cm^{-3}$. The doping in body and S/D region was uniformly doped throughout the device. Aluminium metal gate of low contact resistivity was used as gate of the device. Nitride spacer was introduced across the uncovered fins of the raised source/drain device. The 3-D TCAD Synopsys tool was used to implement the device. The structure of $In_{0.53}Ga_{0.47}As$ FinFET is shown in Figure **1**(a) while Figure **1**(b) demonstrates the cross sectional view of the FinFET.

Table 1: Parameters used in the structure

Variable	Symbol	Value
Gate Length	L_g	14 nm
Gate Oxide Thickness	T_{ox}	2.78 nm
Dielectric Constant		25 pF/m
Fin Doping	N_{ch}	$10^{17}cm^{-3}$
Fin Height	H_{fin}	21.25 nm
Fin Width	W_{fin}	8.5 nm
S/D-HDD Doping	N_{HDD}	$5x10^{19}cm^{-3}$
Gate Extension	G_{fin}	50 nm
Thickness of Gate Poly	T_{gate}	32 nm

Thickness of Metal Contact	T_{metal}	30 nm
Extended fin Length	L_{ext}	20 nm

3-D TCAD Synopsys tool was used to design and simulate the device. The framework of device physics used for the simulating 14 nm channel length FinFETs had been incorporated by calibrating the experimental device of 50 nm channel length $In_{0.53}Ga_{0.47}As$ nFinFET [11]. The state of art is similar to that adopted in [12]. The device physics models used in calibrating the 50 nm channel length by including quantization effects and non parabolicity effects for sub-14 nm $In_{0.53}Ga_{0.47}As$ nFinFETs to take care of quantum confinement effects. The energy bandgap relations and the band structure of InGaAs that exhibit non-parabolic behaviour at various valleys were also considered in the device. The Lombardi mobility model, ShockleyReadHall, Hurkxx Auger, quantum corrected drift-diffusion, density gradient, Fermi-Dirac statistic, models have been used for simulation of 14 nm channel length $In_{0.53}Ga_{0.47}As$ FinFETs to obtain various performance parameters of the device. The framework of device physics used for the simulating 14 nm channel length FinFETs has been incorporated by various physics models adopted in [12]. The experimental device of 50 nm channel length $In_{0.53}Ga_{0.47}As$ nFinFET was calibrated with the help of the drift diffusion model and I_{ds}-V_{gs}. The I_{ds}-V_{ds} characteristics have been shown in Figure **2**.



(a) (b)

Figure 2: Calibration of $In_{0.53}Ga_{0.47}As$ nFinFET with L_g= 50 nm (a)I_{ds}-V_{gs} transfer characteristics during different drain bias (b)I_{ds}-V_{ds} output characteristics during different gate bias.

3. METHODS

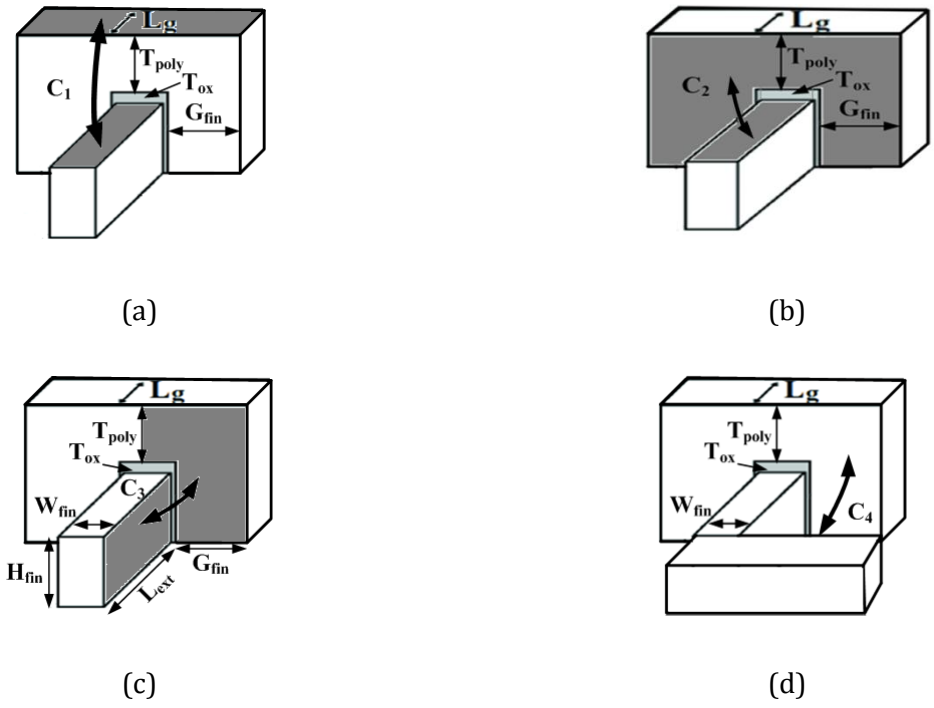


Figure 3: Gate Parasitic Capacitance (a) Parasitic Capacitance C_1 at top of gate gate and top of the fin (b) Parasitic Capacitance C_2 at gate sidewall and top of the fin (c) Parasitic Capacitance at C_3 gate sidewall and fin sidewall (d) Parasitic Capacitance C_4 at gate sidewall and S/D sidewall.

The $In_{0.53}Ga_{0.47}As$ FinFET has several parasitic components among which the gate parasitic capacitance is important constraint for the analysis and the performance of the device and it also affects equivalent gate capacitance of FinFET.

3.1 Gate Parasitic Capacitance

Figure **3** shows various parasitic capacitances attached with gate. The delay of the device is dependent on gate capacitance of the device indulging the gate parasitic capacitance which decreases the overall performance of the device. Hence, parasitic gate capacitance in $In_{0.53}Ga_{0.47}As$ channel will also have a significant effect. The gate parasitic capacitances are divided into four components: (i) Top of gate and top of the fin C_1 (ii) Gate sidewall and top of the fin C_2 (iii) Gate sidewall and fin sidewall C_3 (iv) Gate sidewall and S/D sidewall C_4. Figure **3** shows all the parasitic capacitance observed due to gate.

C_1 is the fringing parasitic capacitance at top of gate and top of the fin as shown in Figure **3**(a). The model is derived by Wu and Chan [6] and given by eq.(1).

$$C_1 = \frac{2\epsilon_{ox}(W_{fin} + G_{fin})}{\pi} ln\left(\frac{T_{gate} + T_{ox} + L_g}{T_{gate} + T_{ox}}\right) \quad (1)$$

Where, ε_{ox} is dielectric constant of oxide, G_{fin} is extended gate length, T_{gate} is thickness of gate, T_{ox} is oxide thickness and W_{fin} is width of fin. The capacitance model [6] was developed considering Si as fin while, in case of InGaAs fin several parameters got differs so the model too differs in term of parameters.

C_2 is the fringing parasitic capacitance at the gate sidewall and top of the fin as shown in Figure **3**(b). The model for C_2 is derived in [6] and given by eq. (2).

$$C_2 = \frac{2\epsilon_{ox} W_{fin}}{\pi} \times a + \frac{\eta_1 \epsilon_{ox} W_{fin} e^{-1}}{\pi} ln\left(\frac{2\pi W_{fin}}{T_{ox}}\right) \quad (2)$$

$$a = ln\left[\frac{T_{ox} + \eta_2 T_{gate} + \sqrt{(\eta_2 T_{gate})^2 + 2\eta_2 T_{gate} T_{ox}}}{T_{OX}}\right]$$

$$\eta_2 = exp\left[\frac{L_{ext} - \sqrt{(T_{gate})^2 + 2T_{gate} T_{ox}}}{\tau_1 L_{ext}}\right]$$

η1=7.9 τ1=15

Where, L_{ext} is extended fin length and η1, τ1 are the fitting parameters.

C_3 is the fringing parasitic capacitance at gate sidewall and fin sidewall as shown in Figure **3**(c). The model for C_3 is derived in [6] and given by eq. (3).

$$C_3 = \frac{8\epsilon_{ox} H_{fin}}{\pi} \times b + \frac{\eta_4 \epsilon_{ox} 4H_{fin} e^{-1}}{\pi} ln\left(\frac{4\pi H_{fin}}{T_{ox}}\right) \quad (3)$$

$$b = ln\left[\frac{T_{ox} + (\eta_3 G_{fin}/2) + \sqrt{(\eta_3 G_{fin}/2)^2 + 2\eta_2 G_{fin} T_{ox}}}{T_{OX}}\right]$$

$$\eta_3 = exp\left[\frac{L_{ext} - \sqrt{(G_{fin}/2)^2 + G_{fin} T_{ox}}}{\tau_2 L_{ext}}\right]$$

η4=5 τ2=30

Where, η4 and τ2 are the fitting parameters.

C_4 is the capacitance between gate sidewall and S/D sidewall which is represented in Figure **3**(d) and given by eq. (4).

$$C_4 = \frac{H_{fin} G_{fin} \epsilon_{ox}}{L_{ext}} \left(\frac{\tau_3 (G_{fin} + 2T_{ox})}{L_{ext}} + k_1\right) \quad (4)$$

Where, τ_3 and k_1 are fitting parameters and the magnitudes are 3.3568 and 0.0596 respectively, while the overall parasitic capacitance across the gate is given by eq. (5).

$$C_{par} = 2(C_1 + C_2) + 4(C_3 + C_4) \quad (5)$$

The total gate parasitic capacitance consists of total fringing capacitances and other capacitances observed across gate.

3.2 Interface traps in $In_{0.53}Ga_{0.47}As$ FinFET

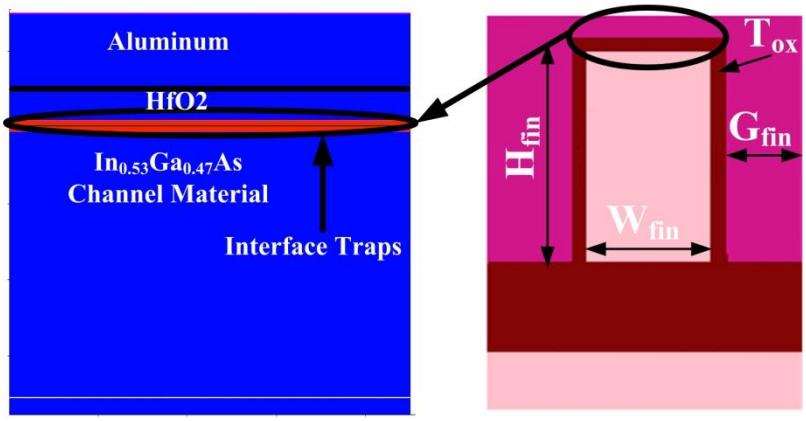
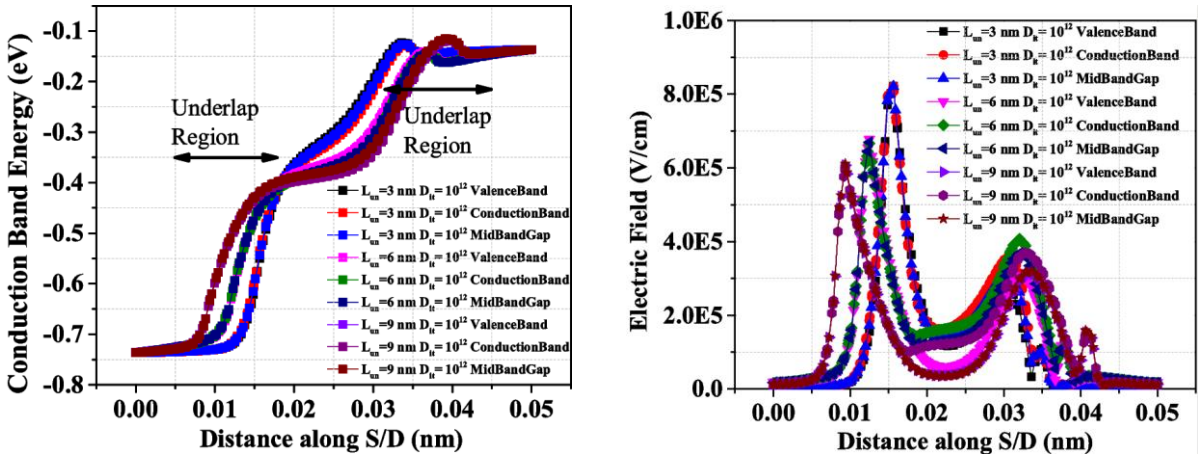


Figure 4: Cross sectional view with interface traps



(a) (b)

Figure 5: Conduction Band Energy and Electric Field for D_{it}= $10^{12}cm^{-2}eV^{-1}$ at different energy trap levels.

The interface traps in $In_{0.53}Ga_{0.47}As$ FinFET may exist as acceptors or donors at interface region. However, in order to understand the interface traps at high-k/InGaAs region the cross-section of FinFET across the oxide/channel should be considered. The cross section would appear as moscap which can be seen in Figure (**4**). In MOS the analysis of interface traps is dependent on the total gate charge across the surface. The charge neutrality in MOS is maintained by charge density across the gate and charge density across the substrate when there are no interface traps ($\Delta Q_g + \Delta Q_s = 0$).On the other hand, in presence of interface traps this charge neutrality gets disturbed which results in the reduced charge density across substrate ($\Delta Q_g + \Delta Q_{it} + \Delta Q_s = 0$). The charge density across the substrate is only responsible for the inversion of channel formation in FinFETs. The impact of acceptor and donor traps for all the underlap devices follows a Gaussian distribution which is considered at the different energy levels. The distribution of traps at different energy levels has provided the significant effects in all the underlap devices. The trap energy levels are distinguished among conduction band energy, mid-band energy and valance band energy. The behaviour of traps at different energy levels can be understood by analysing the electron density, electrostatic potential, electron velocity, electric field and band energy gap across channel and S/D region. Figure **5** shows the conduction band energy and electric field profile across the S/D region for D_{it}= $10^{12}cm^{-2}eV^{-1}$at different trap energy levels.

The electron field at V_{gs}=V_{dd} and V_{ds}=V_{dd} in presence of nitride spacers across S/D region remains unaffected of interface traps at various energy levels. Conduction band energy of different L_{un} also follows a similar phenomenon across S/D region in spite of various energy levels of interface traps.

4. RESULTS AND DISCUSSIONS

The parasitic capacitances observed due to the gate are dependent on many geometrical parameters such as height and width of the fin, extended gate length and extended fin length. The capacitance variation due to the geometry of FinFET provides variation in intrinsic delay of the device etc. So in this section, the variation in gate parasitic capacitance due to the geometry of $In_{0.53}Ga_{0.47}As$ FinFET is analyzed.

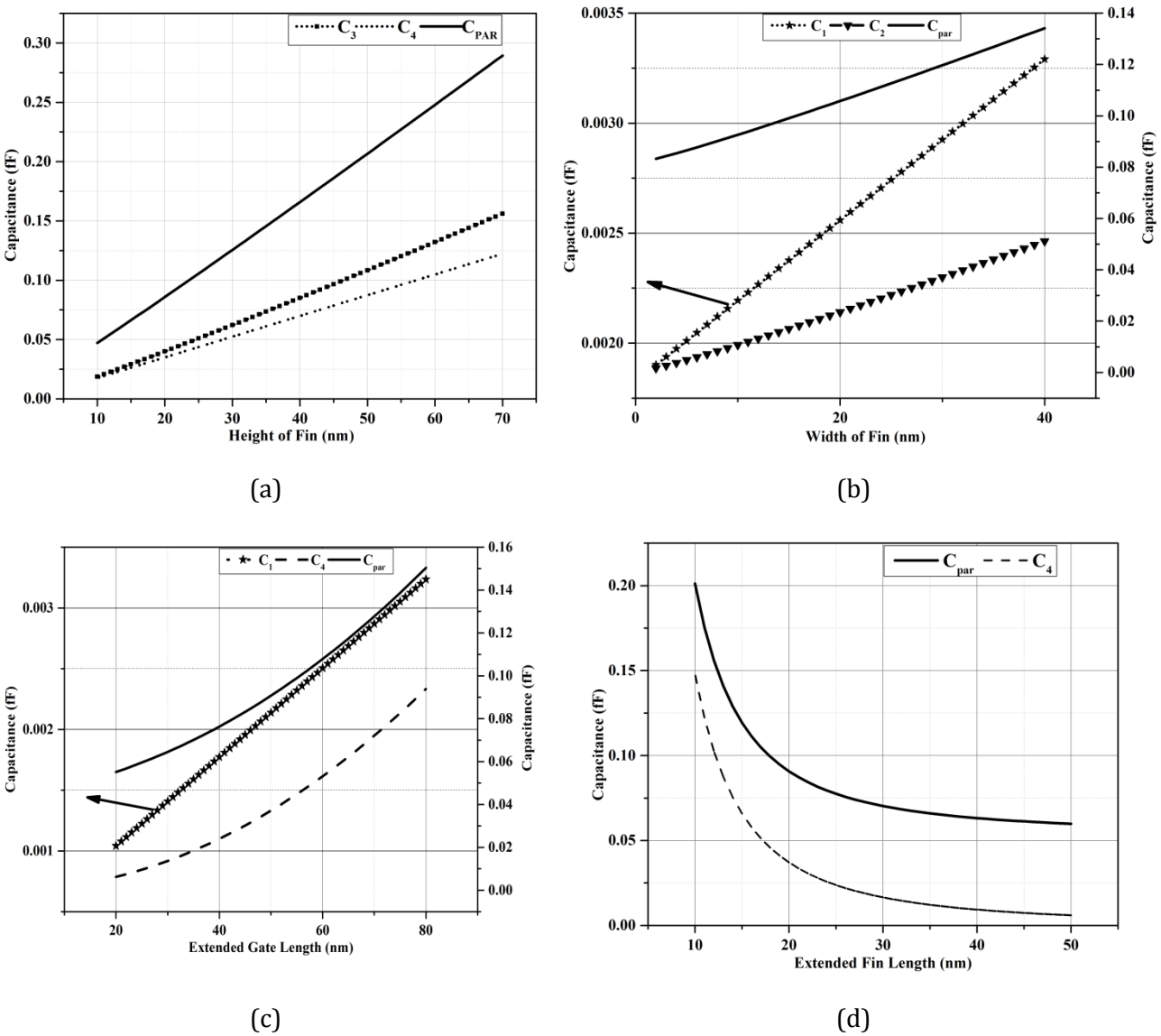
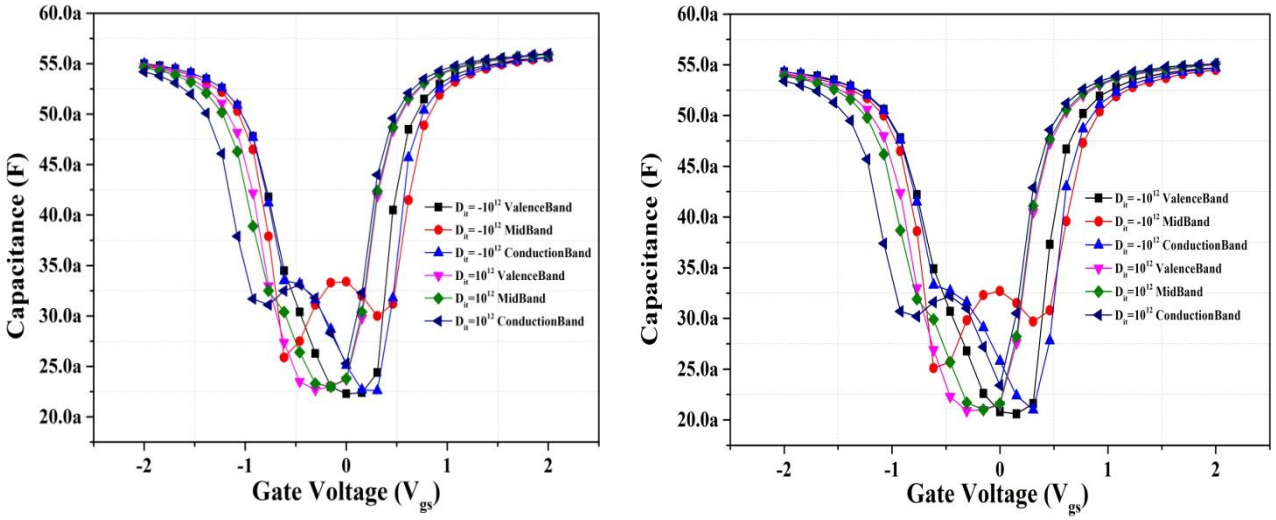


Figure 6: Gate Parasitic Capacitance (a) Parasitic Capacitance versus Height of fin (b) Parasitic Capacitance versus Width of fin (c) Parasitic Capacitance versus Extended Gate Length (d) Parasitic Capacitance versus Extended fin Length

Figure **6**(a) shows the dependence of height of fin on the parasitic capacitance. The capacitances C_3 and C_4 increase while other capacitances C_1 and C_2 are unaffected with the increase in H_{fin}. The variation in C_3 and C_4 provides a change in overall parasitic capacitance C_{par} due to which it also increases withH_{fin}. The capacitance C_3 is present due to fin sidewall hence H_{fin} affects its capacitance, while C_4 is due to S/D sidewall as the height of S/D region is considered to be equivalent to that of H_{fin}

so the capacitance gets affected. Figure **6**(b) shows variation in gate parasitic capacitance with respect to the width of fin. The capacitances C_1 and C_2 increase with W_{fin}, while other capacitances are unaffected. The variation in this capacitance also influences the overall parasitic capacitance C_{par}. The change in both parasitic capacitance C_1 and C_2 can be explained as both the capacitances are present due to top of fin, so increasing W_{fin}will increase the overall plain surface resulting in the increase in capacitance. Figure **6**(c) shows the effect of extended gate length on the gate parasitic capacitance. The capacitances C_1 and C_4 are affected only when G_{fin} increases, as a result, the overall parasitic capacitance increases. The change in C_1 and C_4 is due to the gate sidewall which is the side part of gate i.eG_{fin}. When multiple fins are considered the parasitic capacitance is more influenced by G_{fin}. Figure **6**(d) shows the influence of extended fin length on gate parasitic capacitance. On increasing L_{ext} only the capacitance C_4 is affected as no substantial variation is observed for other capacitances This variation affects the overall parasitic capacitance as L_{ext} increases. The parameter L_{ext} improves the subthreshold slope and DIBL of the FinFET but it still affects parasitic capacitance. The length between the channel and S/D region is increased so the overall parasitic capacitance reduces. The geometrical parameters which have been seen earlier affects gate parasitic capacitance. The influence of all these capacitances have a major impact on the overall gate capacitance which can later increase or decrease the delay of the device.

The C-V characterization of devices, as shown in Figure**7** was performed using Sentaraus TCAD [1]. The C-V characteristics of two different devices with L_{un}= 6 nm and 9 nm have been analysed. The acceptor type and donor type of interface traps were considered with D_{it}= $10^{12}cm^{-2}eV^{-1}$ The Gaussian distribution of traps was considered at the different energy level. Figure **7** reflects the effect of acceptor and donor traps impact on C-V characteristics. When he impact of traps(acceptor or donor) was concentrated at Mid Band Gap,a change in C-V characteristics is observed. The stiff hump is observed across the flat band voltage. The extra trap charges during depletion region allow breaking the depleted barrier across the flat band voltage and results in the formation of extra carrier charges. These carrier charges create hump during the low-frequency operation. When the acceptor trapcharges are at conduction band the C-V curve shifts towards right. Alternatively, when donor traps are at valence band the C-V curve shifts towards left..



(a) (b)

Figure 7: Gate Capacitance for InGaAsFinFET with D_{it}= $10^{12}cm^{-2}eV^{-1}$ (a)L_{un}= 6 nm (b)L_{un}= 9 nm

Table 2: Performance Comparison for all the underlap Devices

Underlap Length	Energy Band Gap	Traps	I_{dsat}	DIBL (V/V)	SS (mV/decade)	Cap(F)	Delay(s)
L_{un}=3nm	Mid band	Acceptor	4.606	0.283	146	5.39E-17	7.02E-12

		Donor	5.546	0.315	143	5.39E-17	5.83E-12
	Conduction band	Acceptor	5.07	0.29	153	5.39E-17	6.38E-12
		Donor	5.074	0.298	145	5.39E-17	6.37E-12
	Valence band	Acceptor	5.05	0.313	144	5.38E-17	6.39E-12
		Donor	5.09	0.289	145	5.10E-17	6.017E-12
L_{un}=6nm	Mid band	Acceptor	3.32	0.258	91	5.50E-17	9.94E-12
		Donor	3.99	0.284	93	5.47E-17	8.23E-12
	Conduction band	Acceptor	3.36	0.25	95	5.48E-17	9.785E-12
		Donor	3.65	0.26	96	5.46E-17	8.97E-12
	Valence band	Acceptor	3.6	0.268	93	5.50E-17	9.17E-12
		Donor	3.66	0.288	93	5.42E-17	8.89E-12
L_{un}=9nm	Mid band	Acceptor	2.519	0.273	83	5.43E-17	1.293E-11
		Donor	3.08	0.27	88	5.40E-17	1.05E-11
	Conduction band	Acceptor	2.79	0.22	83	5.41E-17	1.163E-11
		Donor	2.8	0.26	87	5.39E-17	1.155E-11
	Valence band	Acceptor	2.78	0.262	86	5.43E-17	1.172E-11
		Donor	2.81	0.267	85	5.34E-17	1.140E-11

Table2 demonstrates various figures of merit of the devices in presence of acceptor and donor types of interface traps. Interface traps (acceptor or donor) at Mid Band Gap level have a significant effect on I_{dsat} of $In_{0.53}Ga_{0.47}As$nFinFET with L_{un}= 3 nm, 6 nm and 9 nm. The variation in I_{dsat} is approximately 17% when the traps are at Mid Band Gap for L_{un}= 3 nm. Several SCEs like SS and DIBL are also affected when the traps are located at Mid Band Gap. Also, the intrinsic delay of devices in presence of acceptor traps is higher as compared to the donor traps at Mid Band Gap level. Intrinsic delay is highest for L_{un}= 3 nm, 6 nm and 9 nm i.e., 7.02 ps, 9.94 ps and 12.93 ps respectively when acceptor type of traps is at Mid Band Gap level. However, the traps (acceptor or donor) at conduction Band gap and Valence band Gap have no such variation in I_{dsat}, SS, DIBL and intrinsic delay. The interface traps as explained before provides several unwanted effects which may damage the device. Therefore, to overcome the damage several techniques are used like cleaning effect of trimethylaluminum (TMA) on InGaAs surfaces [144], sulphur passivizationon InGaAs MOS at interface properties [15].

5. CONCLUSION

The effect of gate parasitic capacitance is based on the geometry of $In_{0.53}Ga_{0.47}As$ FinFET. The parasitic capacitances observed are generally of fringing capacitance due to the gate. To reduce the effect of gate parasitic capacitance, the optimization of device geometry is required in FinFET. The capacitances are dependent on the height of fin, width of fin, extended gate length etc. Variation in these parameters results into the performance alteration of the $In_{0.53}Ga_{0.47}As$ FinFET. The good mobility of III-V materials improves delay of a device but such gate parasitic capacitance affects delay and the performance of device becomes unfavourable. By optimizing the geometry of $In_{0.53}Ga_{0.47}As$ FinFET the parasitic capacitances can be reduced. The impact of interface traps is generally seen at the interface region of oxide/ $In_{0.53}Ga_{0.47}As$ in InGaAs based FinFET. The interface traps in FinFET device have severe effects mainly in gate capacitance, on current, subthreshold swing, intrinsic delay, off current of the devices.. The traps located at Mid Band Gap affects severely in the performance of the device irrespective of the type of traps. The variation in I_{dsat} due to traps in mid band gap is 17%. A similar impact is seen in other performance parameters of the devices. Hence, traps in mid band gap play an active role when the device is operating in inversion mode. The reduction in interface charges is possible by changing oxides or through fabrication techniques across the oxide/ $In_{0.53}Ga_{0.47}As$ interface.

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